WHAT IS CLAIMED IS:

1. A thin film transistor display comprising:

a driving circuit comprising a first thin film transistor structure, said first thin film transistor structure comprising a first gate, source and drain regions, a first LDD region, a second LDD region and a first channel region between said first and said second LDD regions, said first gate region being disposed over said first channel region and overlapping with said first and said second LDD regions; and

an active matrix controlled by said driving circuit and comprising a second thin film transistor structure, said second thin film transistor structure comprising a second gate, source and drain regions, a third LDD region, a fourth LDD region and a second channel region between said third and said fourth LDD regions, said second gate region being disposed over said second channel region and overlapping with neither of said first and said second LDD regions.

2. The thin film transistor display according to claim 1 wherein the length of said first gate region is greater than said first channel region.

3. The thin film transistor display according to claim 1 wherein the length of said second gate region is no greater than said second channel region.

4. The thin film transistor display according to claim 3 wherein the length of said second gate region is substantially identical to said second channel region.

5. The thin film transistor display according to claim 1 wherein said active matrix and said driving circuit are formed on the same substrate.

6. The thin film transistor display according to claim 5 wherein said substrate is a glass substrate.

7. The thin film transistor display according to claim 1 wherein said display is a liquid crystal display.

8. The thin film transistor display according to claim 1 further comprising:

a passivation layer overlying said first and said second thin film transistor structures; and

a plurality of contact plugs extending from said source/drain regions, respectively.

9. A process for producing a thin film transistor display comprising steps of:

providing a substrate;

forming a polysilicon layer on said substrate;

patterning said polysilicon layer to define a first and a second TFT regions;

providing a first and a second doping masks on said polysilicon layer in said first and said second TFT regions to result in a first exposed portion in said first TFT region and a second exposed portion in said second TFT region;

implanting a first doping material into said first and said second exposed portions, thereby defining a first doped region and a first channel region adjacent to said first doped region in said first TFT region, and a second doped region and a second channel region adjacent to said second doped region in said second TFT region;

removing said first doping mask;

providing a third doping mask on said first channel region, which partially overlies said first doped region, so as to result in a third exposed portion in said first TFT region smaller than said first exposed portion;

implanting a second doping material into said third exposed portions to form first source/drain regions and simultaneously define a first LDD region;

removing said second and said third doping masks;

forming an insulator layer and a gate metal layer on the resulting structure; and

patterning said gate metal layer to form a first and a second gate structures over said first and said second channel regions, respectively,

wherein in a certain direction, said first gate structure is longer than said first channel, and said second gate structure has length no greater than the length of said second channel region.

10. The process according to claim 9 wherein the length of said second gate structure is substantially identical to the length of said second channel region in said certain direction.

11. The process according to claim 9 wherein said first, said second and said third doping masks are photoresists.

12. The process according to claim 9 further comprising a step of doping said patterned polysilicon layer in order to define said first and second TFT regions.

13. The process according to claim 9 further comprising a step of implanting a third doping material into said second TFT region with said second gate structure serving as a doping mask to form second source/drain regions and a second LDD region.

14. The process according to claim 9 further comprising a step of covering a portion of said patterned polysilicon layer with a fourth doping mask before doping said patterned polysilicon layer for further defining a third TFT region.

15. The process according to claim 14 wherein said first TFT region is an N-channel TFT region of a driving circuit, said second TFT region is an N-channel TFT region of an active matrix, and said third TFT region is a P-channel TFT region.

16. The process according to claim 15 wherein said fourth doping mask is removed along with said second and said third doping masks.

17. The process according to claim 16 further comprising steps of:

forming a third gate structure over said third TFT region at the same time when said first and said second gate structures are formed; and

implanting a third doping material into said third TFT region with said third

gate region serving as a mask to form source/drain regions of said third TFT region.